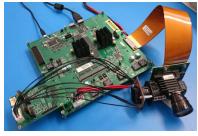
A Full-Color Single-Chip-DLP Projector with an Embedded 2400-fps Homography Warping Engine

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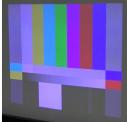






Figure 1: (L to R) Appearance of the projector system; Projected ARIB STD-B28 color bar; Projected image warped by hand gesture; Vision-based tracking projection onto a markerless surface.

ABSTRACT

We demonstrate a 24-bit full-color projector that achieves over 2400-fps motion adaptability to a fast moving planar surface using single-chip DLP technology, which will be useful for projection mapping applications in highly dynamic scenes. The projector can be interfaced with a host PC via standard HDMI and USB without need of high computational burden.

CCS CONCEPTS

Hardware → Displays and imagers;
Computing methodologies → Mixed / augmented reality;

KEYWORDS

high-speed projection, video mapping, stabilized projection

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1 INTRODUCTION

One of key challenges in projection-based interaction systems is adaptability to quick real-world motion. High-frame-rate DLP (Digital Light Processing) projectors, possibly with fast sensory feedback, have been applied to enabling such objectives [Kagami and Hashimoto 2015; Watanabe et al. 2015]. Similar DLP systems have

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also been studied for optical see-through displays [Lincoln et al. 2016; Zheng et al. 2014] and stylus-interaction displays [Ng et al. 2014] for the sake of low latencies. However, none of them presented detailed investigations on projection of color images.

A straightforward way of extending them for color displaying is to employ the "3-chip DLP" configuration where three DMDs (Digital Micromirror Devices) corresponding to the three color channels are incorporated. This configuration is ideal in terms of performance, but increases the hardware cost, making it unsuitable for consumer equipments.

In this study, we explore a single-chip DLP configuration to achieve full-color projection, while maintaining fast adaptability to quick motion of real-world surfaces. We extend our own prior work [Kagami and Hashimoto 2015] to enable color projection considering peculiar issues in single-chip DLP systems. The developed projector applies over 2400 homography transformations per second to video-rate input images from an HDMI interface, which is also a new feature, or a local SDRAM storage.

2 FULL-COLOR MOTION-ADAPTIVE PROJECTION

A DLP projector uses a DMD as a reflective spatial light modulator to produce monochrome binary images at a rate of tens of kHz. Fast modulated light from the projector is time-averaged by human eyes and perceived as gray-level images. With a light source having a constant intensity, it requires 255 binary frames to represent 8-bit gray levels in the PWM (Pulse Width Modulation) encoding.

If one can modulate the brightness of the light source in a frame-by-frame manner, the necessary number of binary frames is greatly reduced. For example, if the ratio of the light source intensity to its maximum, or equivalently the ratio of the illumination period to the binary frame period, can be set at eight different levels $(1,\frac{1}{2},\frac{1}{4},\frac{1}{8},\frac{1}{16},\frac{1}{32},\frac{1}{64},\frac{1}{128})$ for consecutive binary frames, an 8-bit gray-level image can be produced out of these eight binary frames

by assigning each bitplane to the binary frame with the corresponding brightness weight [Bimber et al. 2007]. Let us call this the 8-bit 8-tick, or 8b8t encoding. In order to produce full-color images with the single-chip DLP configuration, this 8-frame sequence must be repeated for three color channels. For 1000-fps motion adaptation to be possible, 24-kbps image data bandwidth per pixel will be required (i.e. 24 Gbps for a 1-Mpixel image). A similar approach that encodes 1000-fps monochrome images more efficiently has been demonstrated [Watanabe et al. 2015], but it cannot be adapted directly to the single-chip DLP configuration because it already exhausts the maximum speed of DMD.

In our prior work [Kagami and Hashimoto 2015], we proposed a different approach, which is similar to [Zheng et al. 2014] and [Lincoln et al. 2016] in spirit, but much simpler. Instead of applying motion adaptation to each set of binary frames that constitute a gray-level or color image, our approach is to simply apply motion adaptation to each of single binary frame as soon as motion information is available. As long as the projected content is pursued by human eyes, visual artifacts are suppressed. This means that the unit time period to which motion adaptation is applied is independent of the video frame period, and therefore, independent of whether the source images are monochrome or color. It requires only 1-kbps bandwidth per pixel for 1000-fps motion adaptation. Our implementation is designed for faster motion and offers up to 2470-fps adaptation with 2.5-kbps image data bandwidth per pixel.

Another issue that must be addressed with the single-chip DLP configuration is inefficiency in light utilization. Because switching between the three color light sources must take place, light utilization becomes 1/3 as efficient as with the 3-chip DLP. From this viewpoint, the 8b8t encoding is not favored as it reduces light utilization by another factor of $\frac{1}{8}\sum_{k=0}^{7}2^{-k}\simeq 1/4$. On the other hand, employing the original PWM encoding is not possible for our design, since a full-color video frame occupies $3\times255/2470\simeq0.31$ [s], which will never be perceived as a single image.

We propose another encoding called *8b19t*, in which the 7th, 6th, 5th and 4th bitplanes occupy 8, 4, 2 and 1 binary frames, respectively, and are illuminated by full intensity, while the 3rd, 2nd, 1st and 0th bitplanes occupy 1 binary frame for each, and are illuminated by $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$ and $\frac{1}{16}$ of the full intensity, respectively. This utilizes light 3.3 times as efficiently as the 8b8t encoding does. We also apply the bit splitting technique [Doherty et al. 1999] to the 7th, 6th and 5th bitplanes and permute the frames in the color-channel-major order to suppress visual artifacts. A full-color frame occupies $3 \times 19/2470 \simeq 0.023$ [s], which apparently is short enough to avoid obvious flicker as far as we tested. Note that the supplementary movie does not exactly tell what our bare eyes perceive, and thus demonstration at SIGGRAPH 2018 Emerging Technologies will be an important opportunity.

3 IMPLEMENTATION

Figure 2 shows a block diagram of the developed system. It receives 24-bpp video via HDMI or from the SDRAM local storage. Bitplanes from the video are read out according to sequence instructions stored in SDRAM. Homography warping, specified by the parameters received asynchronously via USB, is applied to the newest bitplane by XILINX XC7K325T FPGA, which is then sent to Texas

Instruments 0.7" XGA DMD. No special communication buses other than HDMI and USB are required on the host computer side. The DMD is illuminated by color LEDs (Luminus SBM40 and LED Engin LZ4-00MD09 have been tested) controlled also by the sequence instructions, and the reflected light is projected through ViaLUX STAR CORE-07 optics. Figure 1 shows the implemented system and projection results.

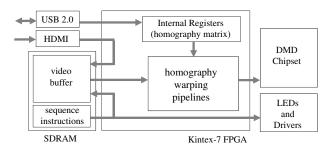


Figure 2: System architecture

ACKNOWLEDGMENTS

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